

NON-VOLATILE SEMICONDUCTOR MEMORY ELEMENT AND CORRESPONDING  
PRODUCTION AND OPERATION METHOD

Inventor(s): SCHULER, et. al.

Attorney Docket No. 10808-205 (In1245/WOUS)

REPLACEMENT DRAWING

1/5

FIG 1 Prior Art

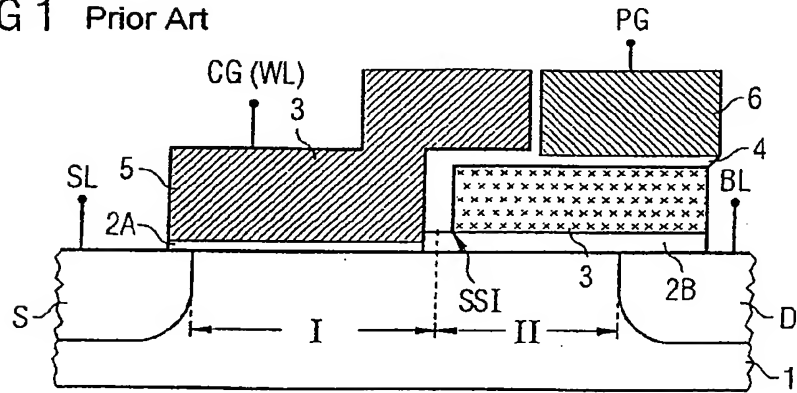


FIG 2 Prior Art

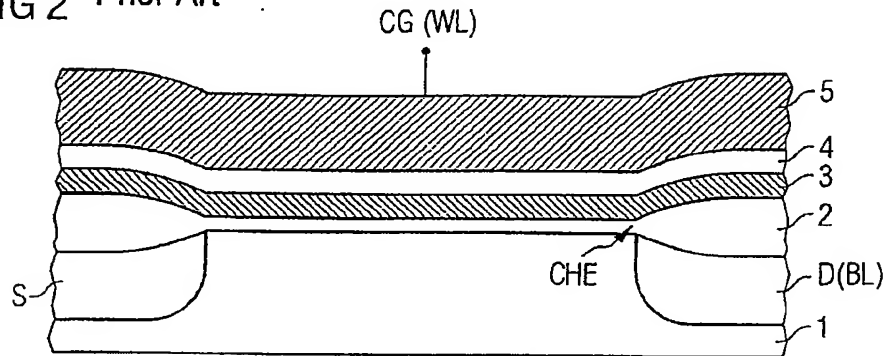
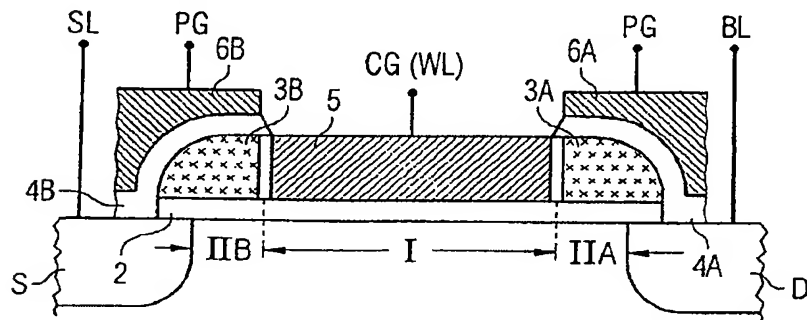


FIG 3 Prior Art



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2/5

A cross-sectional view of a semiconductor device. A central channel region (5) is defined by a central gate (CG (WL)). On either side of the channel are side regions (4A, 4B) and end regions (6A, 6B). The side regions (4A, 4B) are separated from the channel by vertical dividers (4C). The end regions (6A, 6B) are separated from the side regions by vertical dividers (4C). The device is formed on a substrate (S) with a bottom layer (2A, 2B) and a top layer (3A, 3B). The regions are labeled I, II A, and II B. The top layer (3A, 3B) is shown with a hatched pattern. The bottom layer (2A, 2B) is shown with a solid pattern. The central gate (CG (WL)) is shown with a hatched pattern. The side regions (4A, 4B) are shown with a solid pattern. The end regions (6A, 6B) are shown with a hatched pattern. The regions are labeled I, II A, and II B. The top layer (3A, 3B) is shown with a hatched pattern. The bottom layer (2A, 2B) is shown with a solid pattern. The central gate (CG (WL)) is shown with a hatched pattern. The side regions (4A, 4B) are shown with a solid pattern. The end regions (6A, 6B) are shown with a hatched pattern.

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3/5

FIG 6A

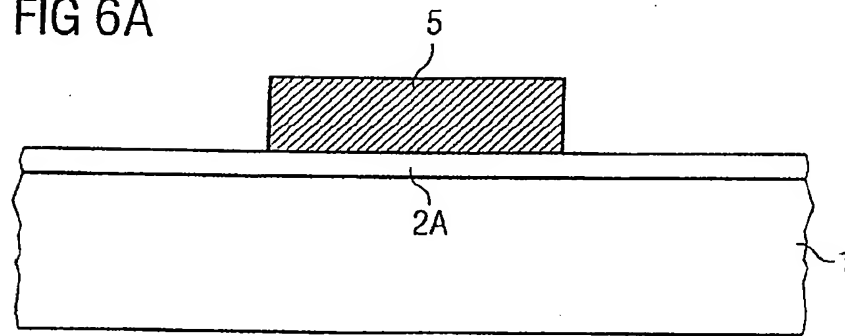


FIG 6B

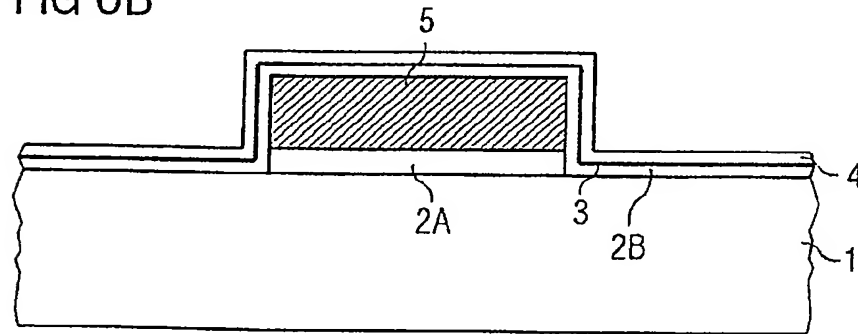
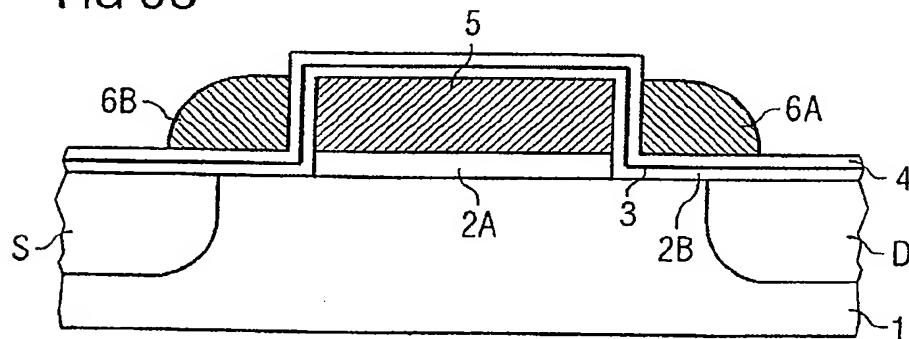


FIG 6C



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4/5

FIG 6D

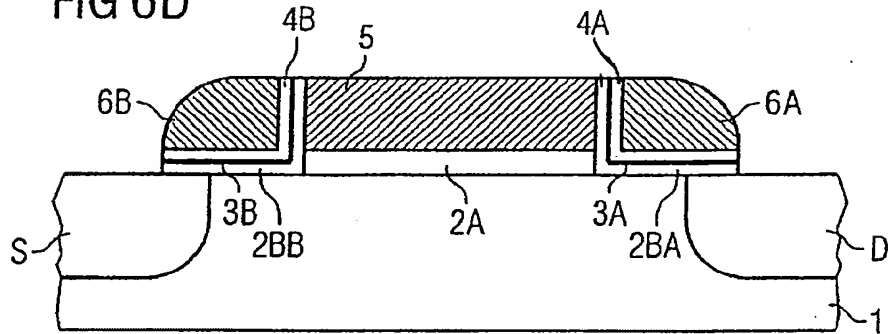


FIG 6E

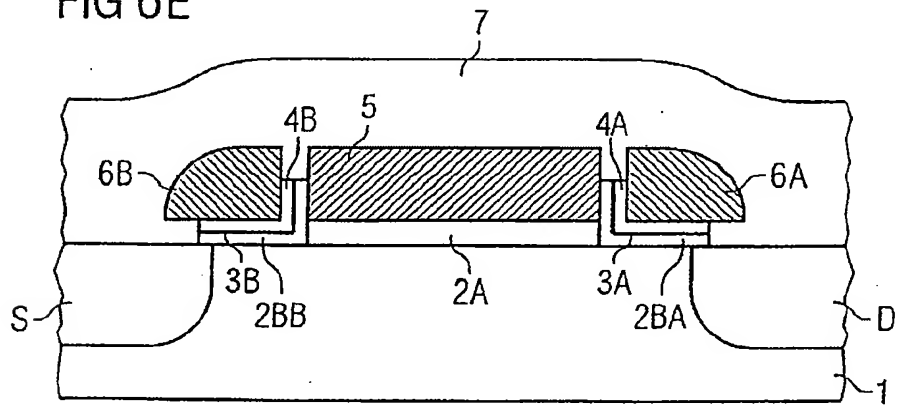


FIG 6F

